JOURNAL OF AERONAUTICAL MATERIALS
ISSN: 1005-5053

Vol. 43, Issue-01, 2023
pp. 396-410

AN EFFICIENT LOW-LEAKAGE FULLY HALF-SELECT-FREE ROBUST SRAM CELLS

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Abstract:

This Project presents two different topologies of 11T SRAM cells with Fully Half-Select-Free Robust operation. The proposed 11T-1 and 11T-2 cells successfully eliminate Read disturb and Write half select disturb and also improve the Write-ability by using power-cutoff. Both the proposed cells successfully eliminate floating node condition encountered in the earlier power-cutoff cells during Write half-select. We also present a comparative analysis of SRAM performance. Here we also calculated Power and Delay values of Proposed SRAM cells.

Keywords: Static Random Access Memory (SRAM), Power cut-off with Floating Avoidance Assist (PCFA), Ground cut-off with Floating Avoidance Assist (GCFA), Column Half Select (CHS).

INTRODUCTION:

With the proliferation in the demand of low power devices like wireless sensor networks, implantable biomedical devices and other battery operated portable devices, power dissipation has become a key design constraint. Static Random Access Memory (SRAM) is the major contributor to the power dissipation, as they occupy significant portion of Systems-on-Chip (SoCs), and their portion will grow further in the future [1]. SRAMs are mainly made up of almost 90% - 95% of VLSI circuits. The main factors such as power consumption, speed and stability have paved the way for various new designs with the objectives of minimizing the power utilization at the low level during write and read operations. Moreover, with the advent of ultra-scaled technologies, the leakage becomes a serious threat. Technology scaling results in a significant increase in leakage currents in CMOS device. Leakage power consumption is a major contributor for power consumption and has become a serious concern in SRAM cells. In the modern technology when the feature size is reduced drastically, supply voltage and threshold voltage must be also reduced in the same pace. The decrease in power supply reduces the power consumption quadratically at the cost of degraded stability and access delay. The cell stability (read stability plus write-ability) in SRAM cell is studied in detail because it is an important design criterion The power consumption will increase as leakage rises exponentially with reduction in threshold voltage (Vth) and gate-oxide thickness [2]. It is, therefore, necessary to minimize the power associated with SRAM in order to have a power efficient design. Reducing the supply voltage is a straight forward way to achieve power efficiency because the active and leakage power reduce quadratically and exponentially respectively with supply voltage [3]. However, at lower supply voltages, process variation severely degrades the performance of SRAM cell [4].

The SRAM cell that we considered in this paper was Proposed 11T SRAM cells which consists of two crossly coupled inverters and access transistors to read and write the data. In case of the SRAM cell the memory built is being stored around the two cross coupled inverters. If we consider that, the input to the first inverter is logic 1 then the output of this inverter will be logic
0. So, after one cycle the output of second inverter will be logic 1. From this we can say that as long as the power is supplied to the SRAM cell logic 1 will be circulated in the inverters. Hence there is no need for periodic refreshing of the circuit. Where as in DRAM the circuit need to be refreshed periodically. SRAM technology is most preferable because of its specifications .Consequently, Read/Write failure probability is significantly increased in the conventional 6T SRAM due to the difficulty in maintaining the device strength ratio in subthreshold region [5]. Researchers have proposed many configurations of SRAM cells [6]-[13] to overcome Read failure by using a separate read buffer. These cells improve the read static noise margin (RSNM) by decoupling the read/write path but still suffer from poor write margin (WM) in the sub threshold region. Also, various write-assist techniques have been described in the literature to increase the write margin of the SRAM cell [14]-[20]. Wordline (WL) boosting [14], [15] and negative bit line (NBL) [16] are the commonly used write-assist techniques for improving the write-ability by strengthening the driving capability of the write access transistor. However, these techniques result in area and power penalties. Weakening the strength of the cross-coupled inverter pair is another useful way of write-ability enhancement. It includes power cut-off [17], [18], raising [19] or floating [11], [20] the cell VSS, etc. Recently, Multi-bit soft error/upset (MCU) has threatened the stability of SRAMs at ultra-scaled technology due to the reduction in effective distance between transistors [21]. Bit interleaving (BI) architectural technique is an efficient way to deal with this error. However, this technique is applicable to the cells, which exhibit fully half-select (HS) free operation. The straight forward approach to achieve HS free operation is to use cross-point cell selection, where write path consists of two access transistors controlled by different row and column based signals [10]. However, stacked transistors in the write access path severely degrade the write-ability, which makes it necessary to use WL boosting for both the row-based and column-based Write WL at the expense of dynamic power.
The two BI cells 11T [17] and 12T [18] were proposed that eliminate HS disturb again by using cross-point selected series connected access transistors. Nevertheless, these cells improve the Write-ability by using
Power Cut off Write-assist and do not require word line boosting; they suffer from degradation of floating-1 level of data storing nodes Q or QB in column write HS cells. They require an extra Pulse-Width-Controller in the column circuitry to achieve very precise pulse width for wordlines during write operation to retain the data in the column write half-select (CHS) cells. Recently, a BI power gated 9T cell [22] has been proposed to solve the HS issue, however the power cut-off used during the write operation again leads to floating of data at storing nodes Q in row half-select (RHS) cells. Therefore, in this work, we propose two new 11T cells that mitigate the HS issue without using write-back or any other assist techniques and support a BI architecture to improve MCU immunity. The first proposed cell (termed as 11T-1) uses supply-cut-off and write '0' only whereas the second proposed cell (termed as 11T-2) uses ground-cut-off and write '1' only technique for write-ability enhancement. The power cut-off in

proposed cells does not lead to floating of data storage nodes in any of the HS cell contrary to the existing 11T [17]

2. PROPOSED SRAM CELLS

2.1 PROPOSED 11T-1 CELL

The schematic diagram of the proposed 11T-1 SRAM cell. The cell core consists of cross coupled inverter with the addition of Power cut-off with floating-avoidance assist (PCFA). The transistors MP1 and MP3 in PCFA network internally cut off the supply voltage to weaken the pull-up path and provide contention-free discharge of the storage node to improve the write-ability. Whereas, transistor MP2, driven by row-based WL avoids the floating-1 situation in CHS cells. The write access transistors MAL and MAR are controlled by column based WLA and WLB signals. Table-I illustrates the status of the control signals in different modes of operation of the proposed cells.

During the Write ‘0’ operation, WLA and WL signals are enabled, whereas WLB and VVSS are disabled. The left inverter is completely cut-off from power supply and node Q is easily discharged through transistors MAL and MR2. Similarly for write ‘1’, the WL and WLB are enabled, whereas WLA is disabled.

Control Signal	Operation			
	Hold	Read	Write ‘0’	Write ‘1’
WLA	0/1	0/1	1	0
WLB	0/1	0/1	0	1
WL	0/1	1/0	1/0	1/0
RBL	1	Pre	0/1	1
RWL	0	1	0	0
VVSS	1	0	0/1	0/1

Table:1 Control Signals & Operations

The supply is now cut-off for right inverter and node QB is discharged easily through MAR and MR2 and consequently ‘1’ is written at node Q. The read operation is accomplished by enabling WL signal and keeping WLA and WLB both at ‘0’. The RBL is pre-charged prior to read operation. The discharging path will be on for RBL through transistors MR1 and MR2 depending on the data stored at QB. The disabled WLA and WLB signals enables complete isolation of data storage nodes (Q and QB) from any read disturbing path during the read access. Therefore, the ‘read upset’ is of no concern even for sub threshold operation. In the Hold Mode, all the control signals are disabled, which provides a completely isolated cross-coupled inverters without any floating node. Therefore, the cell stability in the hold mode is same as 6T cell. The VVSS signal is kept high, which significantly reduces the static power consumption during standby mode.

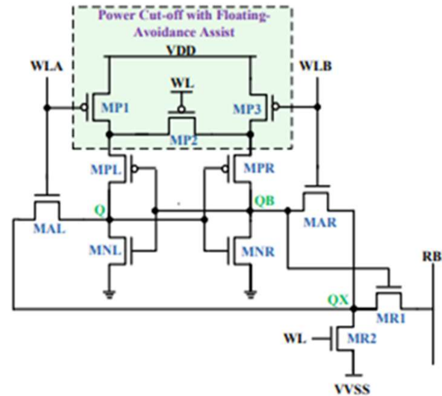

Fig: 2.1 Proposed 11T-1 cell schematics

2.2 PROPOSED 11T-2 CELL

The schematic diagram of the proposed 11T-2 SRAM cell. It consists of the similar cell core with the additional Ground-cut-off with floating avoidance assist (GCFA) comprising of MN1, MN2 and MN3. The transistors MN1 and MN3 in GCFA internally cut-off the ground during write-operation and provide contention free charging of high going node for improving the write-ability. Whereas, transistor MN2, driven by row based WL, prevents the floating-'0' situation in CHS cells. The cell utilizes the single-ended sensing with an additional read buffer comprising of transistors MR1 and MR2. VVSS signal is used to eliminate unnecessary leakage during standby mode. The write access transistors MPAL and MPAR are controlled by column based WLA and WLB signals. Transistor MPU is controlled by row based WL signal, and is shared in a row.

During the Write '0' operation, WLA is enabled, whereas WLB and WL signals are disabled. The right inverter is completely cut-off from ground path and node QB is easily pulled-up through transistors MPAR and MPU without the contention from pull-down transistor MNR. Consequently, Q is discharged to ground through MNL and MN1. The write '1' follows similar procedure due to symmetric write operation.

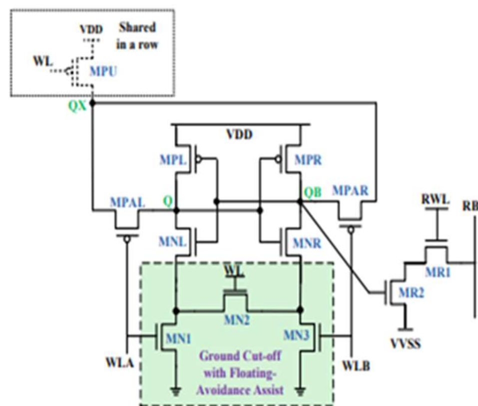

Fig:2.2 Proposed 11T-2 cell schematics.

2.3 WRITE-HALF-SELECT OPERATION OF CELLS

Half-Select disturb is the disturbance caused in storage node of any of the unselected cells in selected rows or column during write operation. HS free operation is necessary for the SRAM cell to be implemented in BI architecture, which is used to solve multi-bit errors. In BI

technique, only one bit of a word is placed at a particular location rather than all the bits of a word together. Thus, even when, data upset occurs at multiple bits locally, it is equivalent to single bit-error in different words, which can easily be recovered by conventional Error correction code (ECC). The proposed 11T cells fully eliminate the HS issue and also prevent the floating node condition of the storage nodes as explained here.

2.3.1 Previous power cut-off 11T cell:

The previous 11T cell [17] uses the cross-point addressed write access to eliminate write HS disturb. Fig. 3.3 shows the CHS cell under write '1' operation. The power cut-off switches, MP3 of the CHS cells will also be turned off. If QB stores '0', it would safely maintain it. However, if QB is storing '1', it will become floating and the voltage level will start to degrade. This problem of floating node will be much severe under parameter fluctuation at low supply voltages and may lead to flipping of data. The simulated transient waveform of CHS cells of various SRAM cells with 5,000 run of Monte- Carlo simulation at TT, 25°C (simulation is performed for 16nm CMOS predictive technology model [24]).

Similarly under write '0' operation, MP4 of CHS cell will be off and node Q suffers from floating-'1' situation. However, the voltage level decrease at node Q will be relatively slower because node R is also being pulled up by MN7 due to high voltage level of VVSS. Therefore, in this case, the data retention time, which is the time up to which the nodes can retain data without flipping, will be relatively longer. In Figure, it is shown that, in the CHS cell of 11T cell [17], floating nodes for the case of Q=1 and Q=0, both are not recoverable and lead to flipping of data. Therefore, for this cell, robust operation of CHS cells cannot be achieved at nanoscale technologies.

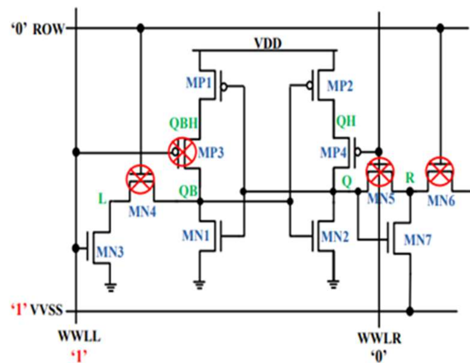

Fig.2.3.1 Column Half-selected cell under write '1' operation for previous power cut-off 11T cell

2.3.2 11T-1 cell:

For RHS cells, the write access transistors in proposed 11T-1 cell are off and cell core is isolated from any disturbing path. Figure shows CHS cell under write '0' operation of 11T-1 cell. The signal WLA is high, whereas WL and WLB are low. The access transistor MR2 is off as WL is '0'. Since MR1 is also off for the case of Q=1, write disturb path does not exist. However, for the case of Q=0, MR1 will be on and Q will be directly accessible to RBL. Still Q will not be disturbed since RBL is also at '0'. Moreover, the PMOS switch MP1 is off, which breaks the pull-up path for left inverter. However, the floating avoidance assist switch, MP2 is on as WL is low, which helps to maintain the pull–up path and avoids floating of Q. Similar operation is observed for write '1' case also due to symmetry of CHS cells in proposed 11T-1.

Fig. 3.5 shows that, floating Q=1 (also QB=1 under write ‘1’ operation) in CHS cell of 11T-1 has been completely recovered and no case of data flip is observed for a run of 5000 MC simulations.

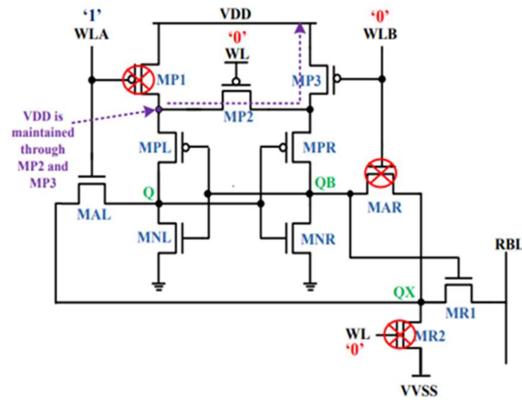

Fig.2.3.2(a) Column Half-select cell under write ‘0’ operation in 11T-1

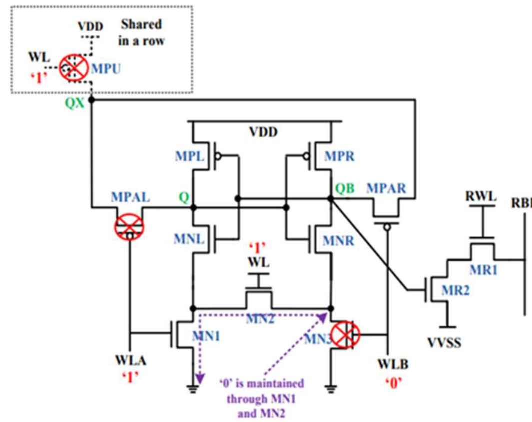

Fig.2.3.3(a) Column Half-select cell under write ‘0’ operation in 11T-2

2.3.3 11T-2 cell:

Similarly, for RHS cells in proposed 11T-2 cell, MPAL and MPAR both are off and cell core is free from any disturbing path. Figure shows CHS cell under write ‘0’ operation of 11T-2 cell. Since MPU is on only for the selected rows, CHS cells will be completely isolated from the write disturb path. WLB is ‘0’, which breaks the pull-down path by turning MN3 off. If QB stores ‘0’, it may float during write access, but floating avoidance switch MN2 helps to maintain the ‘0’ level of the floating node. Similar operation will happen during write ‘1’ operation, where ‘0’ of left inverter is maintained through MN2 and MN3. Figure shows that, floating QB=0 (also Q=0 under write ‘1’ operation) in CHS cell of 11T-2 has been completely recovered and no case of data flip is observed for a run of 5000 MC simulations.

3. DESIGN IMPLEMENTATION

3.1: DESIGN AND IMPLEMENTATION of proposed 11T-1 cell

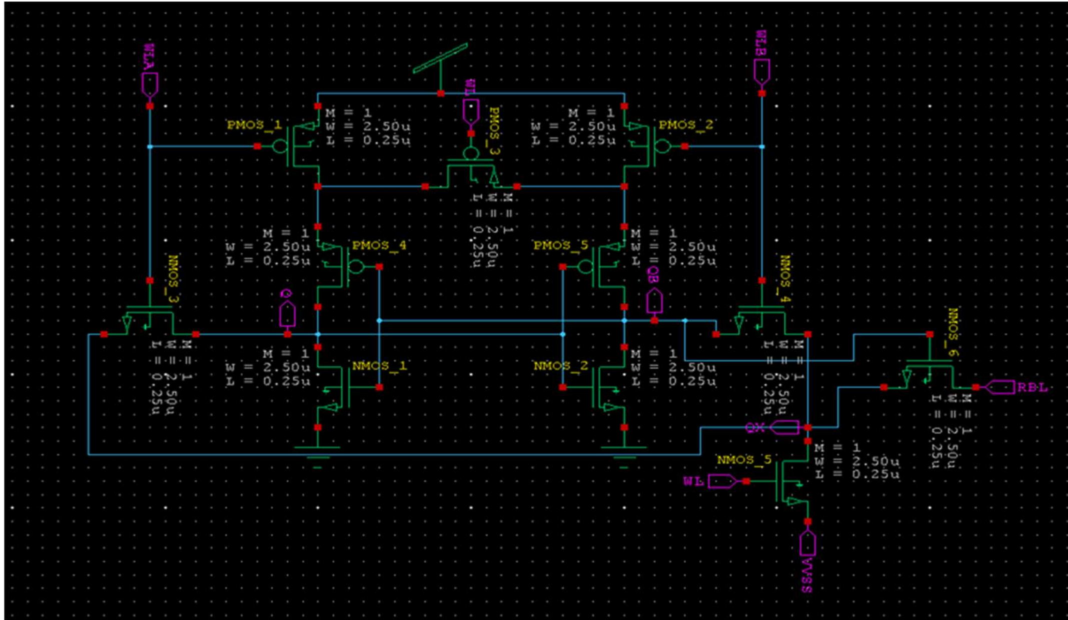

Fig 3.1 Schematic Diagram of 11T-1 Cell

3.2: DESIGN AND IMPLEMENTATION of proposed 11T-2 cell

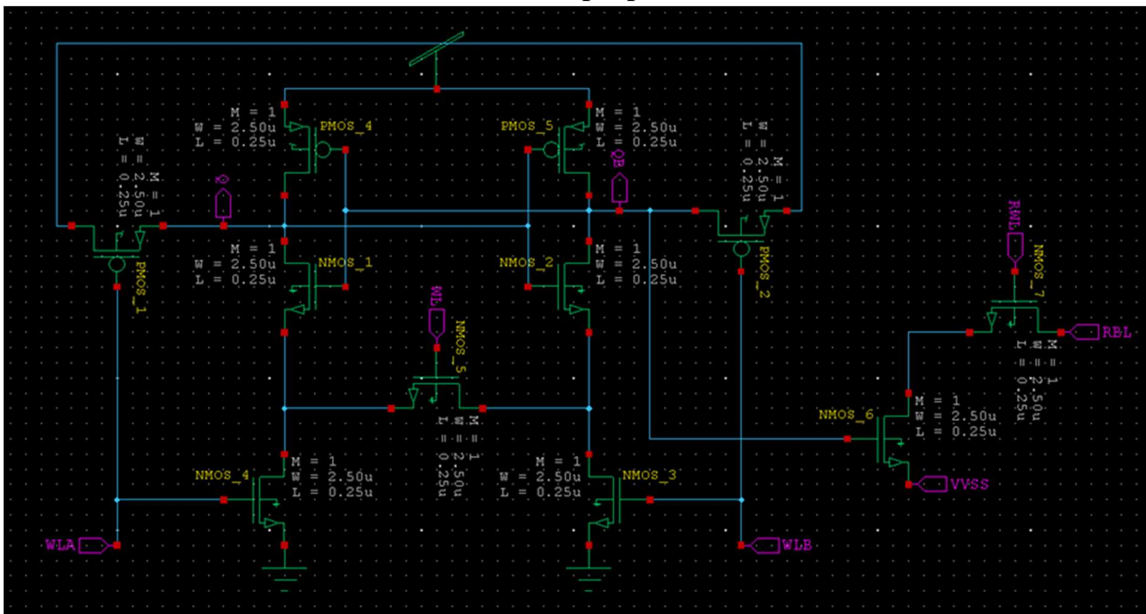

Fig 3.2 Schematic Diagram of 11T-2 Cell

3.3: DESIGN AND IMPLEMENTATION of Column Half-selected cell under write ‘1’ operation for previous power cut-off 11T cell.

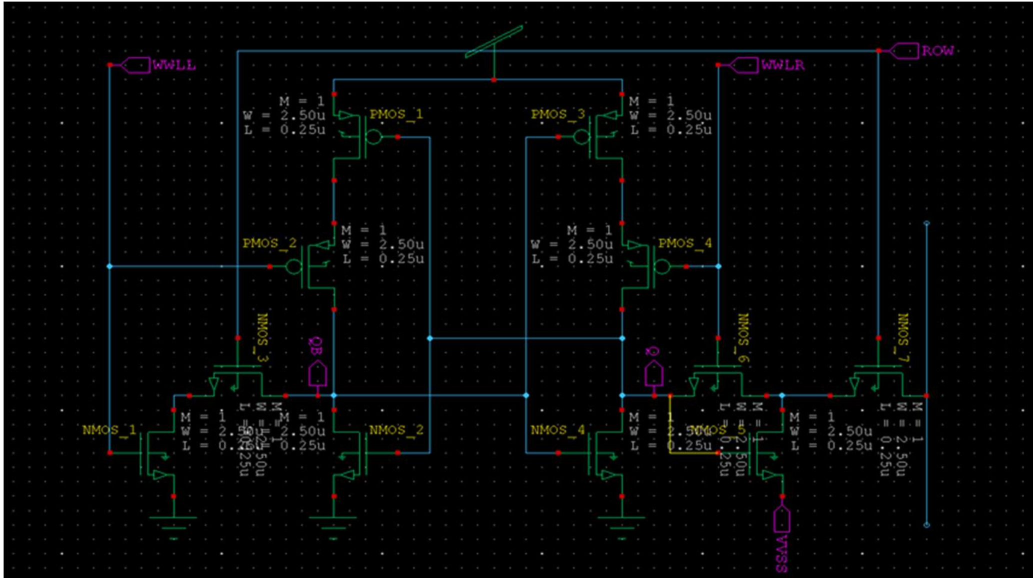

Fig 3.3 Schematic Diagram of Column Half select cell Under Write ‘1’

3.4: DESIGN AND IMPLEMENTATION of Column Half-select cell under write ‘0’ operation in 11T-1 and 11T-2 Cells

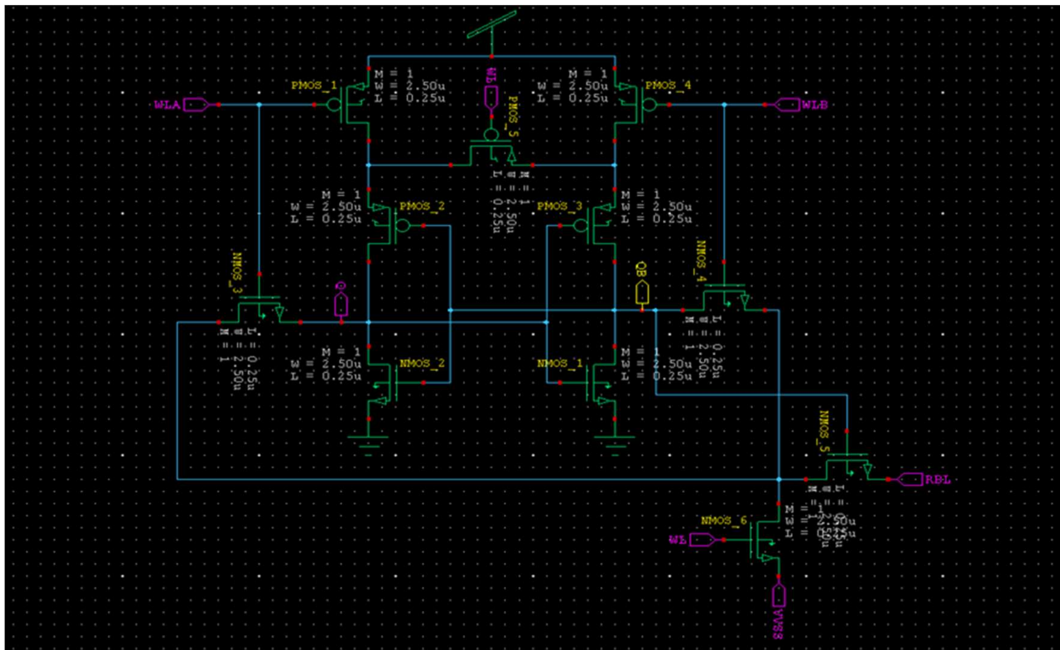

Fig 3.4.1 Schematic of Column Half-select cell under write ‘0’ operation in 11T-1 Cell

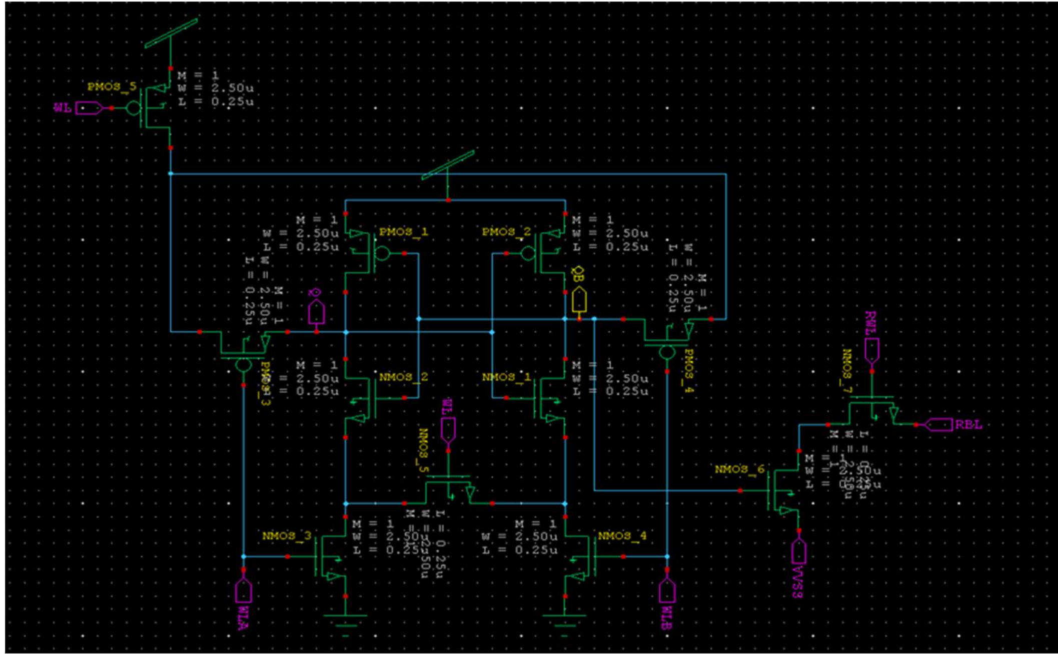

Fig 3.4.2 Schematic of Column Half-select cell under write ‘0’ operation in 11T-2 Cell

4. SIMULATIONS

4.1 : Simulation of Proposed of 11T-1 cell

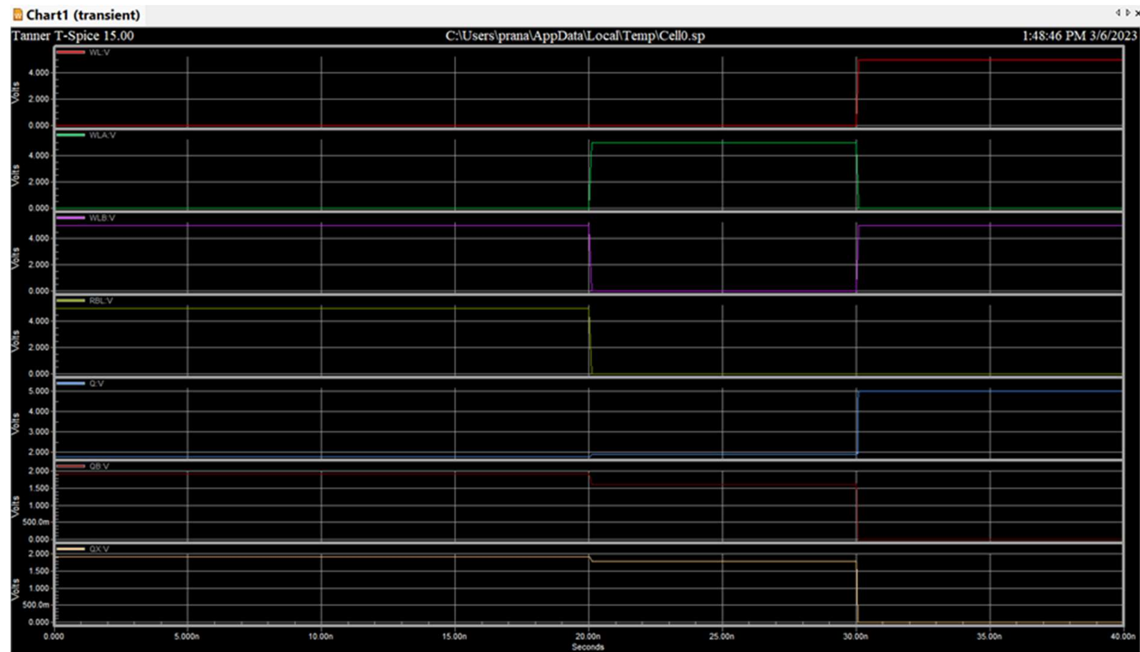

Fig 4.1 Simulation of Pro hkbposed of 11T-1 cell

4.2 : Simulation of Proposed of 11T-2 cell

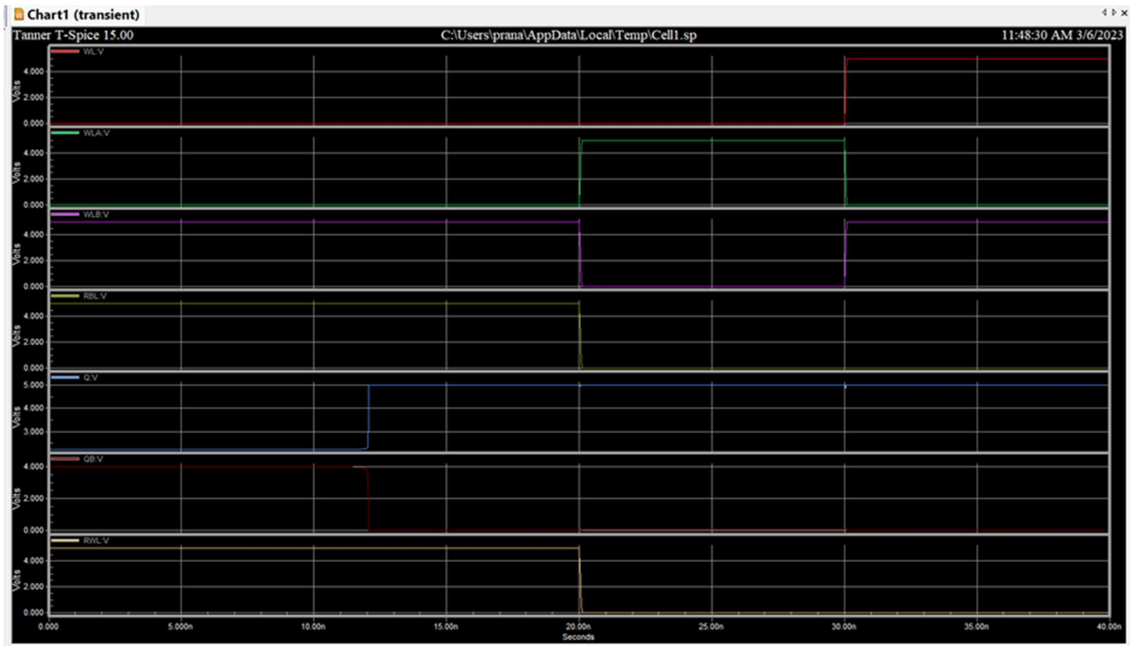

Fig 4.2 Simulation of Proposed of 11T-2 cell

4.3 : Simulation of Proposed of Column Half-selected cell under write '1' operation for previous power cut-off 11T cell

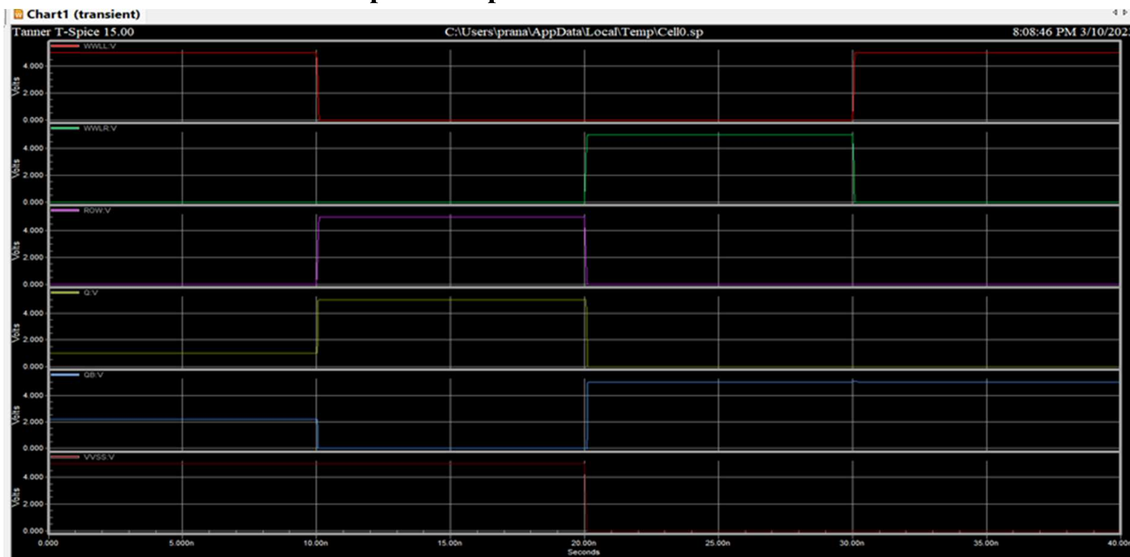

Fig 4.3 Simulation of Column Half select cell Under Write '1'

4.4 : Simulation of Proposed of Column Half-select cell under write '0' operation in 11T-1 and 11T-2 Cells

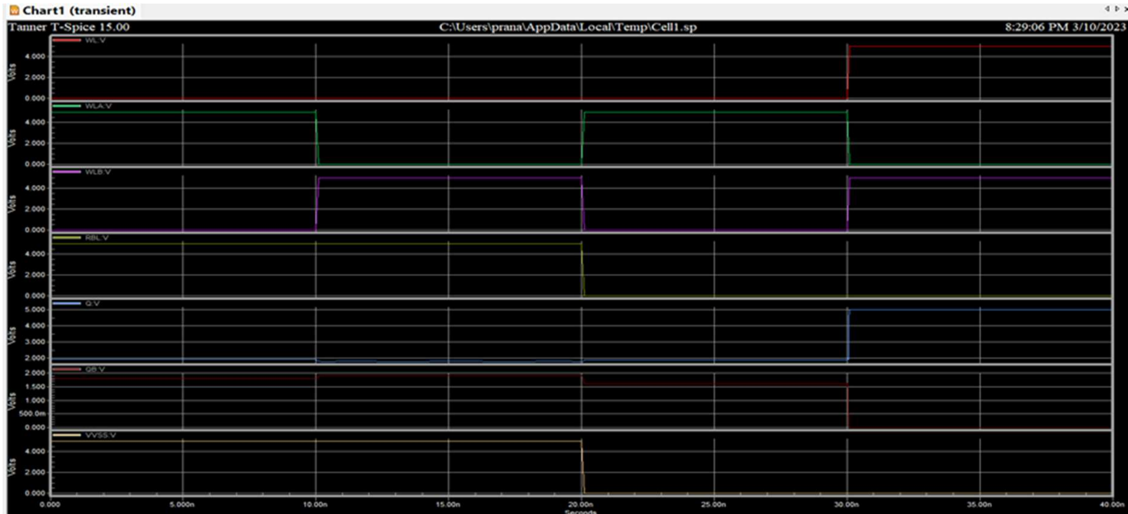

Fig 4.4 Simulation of Column Half-select cell under write '0' operation in 11T-1 Cell

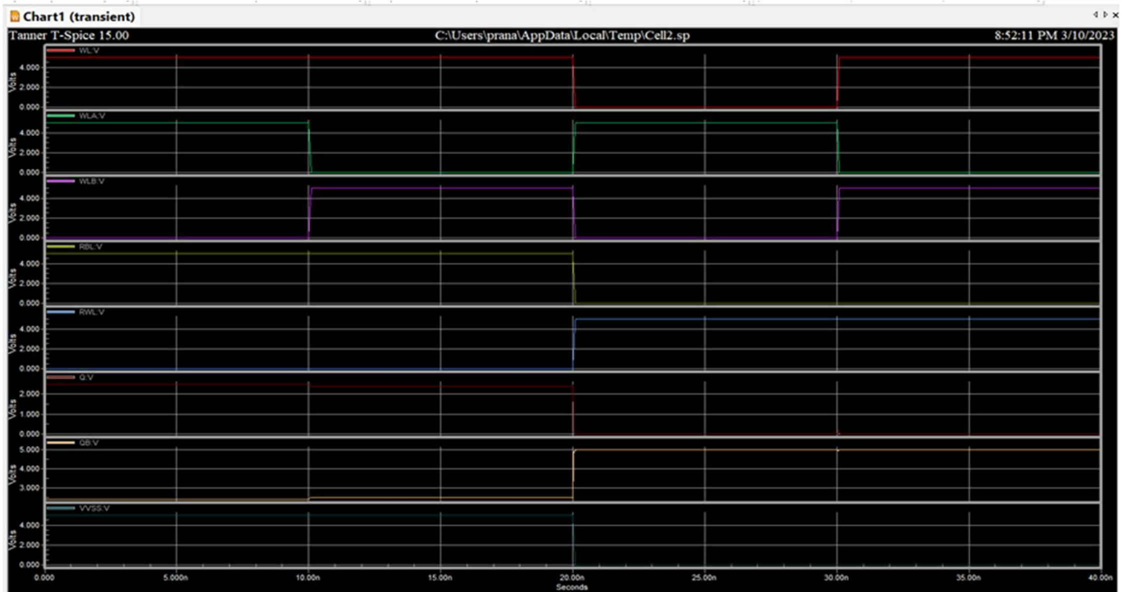

Fig 4.4.1 Simulation of Column Half-select cell under write '0' operation in 11T-1 Cell

5. RESULTS

5.1 POWER AND DELAY CELLS USED

CELLS	POWER (µW)	DELAY (ns)	PDP (µW*n)	TRANSISTOR COUNT
11T-1	0.0925µW	9.958ns	0.9211	11
11T-2	0.0880 µW	9.985ns	0.8786	12
WRITE'0'(11T-1)	0.1454 µW	15.025ns	2.1846	11
WRITE'0'(11T-2)	0.0995 µW	15.025ns	1.4948	12
WRITE'1'11T	0.0950 µW	9.582ns	0.9103	11

Table -2: Power and Delay values

PARAMETERS	**6T**	**7T**	**9T**	**10T**	**11T-1**	**11T-2**	WRITE '0' (11T-1)	WRITE '0' (11T-2)	WRITE '1' (11T)
TRANSISTOR COUNT	6	7	9	10	11	12	11	12	11
WHS FREE	NO	NO	NO	NO	YES	YES	YES	YES	YES
POWER (µW)	0.2623	0.2342	0.2035	0.8262	0.0925	0.0880	0.1454	0.0995	0.0950
DELAY (ns)	10.76	10.57	10.24	10.11	9.958	9.985	15.025	15.025	9.582
PDP (µW*n)	2.822	2.475	2.0838	8.3528	0.9211	0.8786	2.1846	1.4948	0.9103

Table-3: Comparison of proposed 11T cells with previous cells

6. Conclusion

This work proposed two fully half-select-free robust 11T SRAM cell topologies that are suitable for bit-interleaved architecture. The proposed 11T-1 and 11T-2 cells eliminate Read disturb, Write half-select disturb and improves the Write-ability by using power-cutoff and write '0'/ '1' only techniques. The 11T-1 and 11T-2 cells have shown higher read and write yields compared with 6T cell. Both the proposed cells successfully eliminate the floating node condition encountered in earlier power cut-off cells during write half-select. Tanner EDA simulation confirms low voltage operation without any additional peripheral Write - and Read-assist circuits. the proposed 11T cells could be an excellent choice for reliable SRAM design at nanoscale technologies amidst process variations and transistor aging effect.

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